**Q1**: The paper reports on a readout system for an electromagnetic calorimeter based on PIN diodes. It is strongly based on prior work performed within the CALICE collaboration, using their ASIC and a wafer developed by Hamamatsu in the CALICE context. The CALICE publications are quoted, however the relationship should be made more transparent in the introductory part of the paper.

**A1**: This part has been added to the introductory part to stress the relationship with the CALICE collaboration.

“The system is based on the prior work performed within the CALICE collaboration, using their ASIC and referencing to the readout electronics architecture of the CALICE ECAL physics prototype and technical prototype [8,9].”

**Q2**: The hardware configuration, with electronics externally and next to instead of on top of the sensors, may be adequate for system tests, also with particle beams, but it is not really state of the art with respect to the design of detectors for collider experiments. Both the CALICE collaboration and the CMS collaboration are actively pursuing the development of silicon-based calorimeters with integrated read-out-boards interfaced to the silicon sensors within the volume of the detector, which brings considerable additional system challenges. This is not mentioned, either, and should also be discussed in the introduction, or in the conclusion, the claim made in the conclusion that the system is scalable is not valid without these further qualifications

& System is scalable: This is over-selling the results. The system may be scalable to a test beam prototype like the one constructed by CALICE in 2005, but since the electronics is still external and next to instead of on top of the wafer, it is not scalable to a collider detector.

**A2**: It’s true that the conclusion of scalable feature is not valid based on the current system. The main objective of this design is to expand to a testbeam prototype like CALICE ECAL 2005. This part in conclusion has been rewritten.

This system is not really state of the art. But unlike the ILC detector, the CEPC detector will operate in continuous mode, which leads to the fact that the SKIROC2 ASIC is not suitable concerning its power consumption (about 5 mW per channel) and working mode (Acquisition - Conversion - Readout). This system has two main scientific objectives. One is to verify whether the basic performance, such as SNR and resolution, of Silicon PIN diode and ASIC meets the requirements of CEPC ECAL. These features are elaborated in the manuscript. The other objective is to propose an architecture that is easy to expand to a beam prototype. Since the interface protocol for each module has been settled, it is easy to expand to a beam prototype by replacing FEB (with more ASICs and Silicon PIN cells) and DCM (with more optical transceivers). After beam test, specific requirements for new ASIC as well as Silicon PIN diode will be made according to the results.

The elaboration of these two goals has also been added to the introduction and conclusion.

**The introduction part has been rewritten as below:**“To satisfy the requirements mentioned above, a multi-channel readout system is currently being developed to test the performance of silicon PIN diodes and pre-design the prototype for beam test. The system is based on the prior work performed within the CALICE collaboration, using their ASIC and referencing to the readout electronics architecture of the CALICE ECAL physics prototype and technical prototype [8,9]. But unlike the ILC detector, the CEPC detector will operate in continuous mode, which leads to new requirements for the ASIC. One of the two purpose of the system is to verify whether the basic performance of ASIC and silicon PIN cell, such as SNR and range, meets the requirements of the CEPC ECAL. The other purpose is to propose an architecture that is easy expand to a beam prototype. Details of the readout system and preliminary test results are presented below.”

**The conclusion part has been rewritten as this:**

“In this paper, a prototype architecture of readout electronics based on the SKIROC2 for silicon PIN detectors has been presented. It consisted of FEB, DIF and DCM modules. The system was intended to verify if the basic performance of ASIC and silicon PIN cell meets the requirements of Si-W ECAL for CEPC, as well as to explore the design concept of the beam prototype. Since the interface protocol for each module has been settled, it is easy to expand to a beam prototype by replacing FEB and DCM with more silicon PIN cells, ASICs and optical transceivers. The performance assessment of the system with one single layer is discussed in detail. Although the operating mode and power consumption of SKIROC2 did not meet the CEPC requirements, the joint tests with X-ray and cosmic ray showed encouraging results of resolution. This study provides the basis for the implementation of a system with six layers of silicon PIN array and tungsten absorber. In future, it will upgrade to a beam prototype with dozens of layers of silicon PIN diode pad arrays for beam test. After beam test, specific requirements for new ASICs and silicon PIN diode will be put forward according to the results. ”

**Q3:** A large fraction of the paper deals with the read-out chain, including the digital elements for control and data concentration. This hardware is not based on CALICE work but is taken from a different project. However, there are no performance characterizations for a multi-layer system given, only results for single channels or for a single chip at most. There is not even an evidence that the collection of data from several layers worked.

**A3**: Since the main purpose of this manuscript is to pre-design the beam prototype, the main part of the paper, as a result, is about the architecture of readout electronics and the basic performance of the system. Given the fact that the interface protocol worked well with single-layer system and the basic performance was encouraging, we are confident to proceed to next step of designing new version FEB and DCM for beam prototype. As for the data collection of several layers, the key is the transmission data throughput and stability of DCM. These features has been proved enough and elaborated in the referenced paper:

C. Li et al., Design of the FPGA-based gigabit serial link for PandaX-III prototype TPC, Radiation Detection Technology and Methods, 1 (2017) 25

To make it clear, this part is added to the manuscript:

“Since the data throughput from a single DIF to the DCM is 10 Mbit/s, while the transmission to PC is via a gigabit Ethernet cable, so one DCM has potential to support dozens of DIFs by increasing the number of SFPs, without changing the interface protocol.”

**Q4**: Given this, and the fact that there is other work on the characterization of the ASIC published, e.g.:  
Beam test performance of the SKIROC2 ASIC M.S. Amjad (Orsay, LAL) et al.. 2015. 7 pp. Published in Nucl.Instrum.Meth. A778 (2015) 78-84

DOI: 10.1016/j.nima.2014.12.011  
Performance study of SKIROC2/A ASIC for ILD Si-W ECAL T. Suehara (Kyushu U., Fukuoka (main)) et al.. Jan 6, 2018. 6 pp. Published in JINST 13 (2018) no.03, C03015  
DOI: 10.1088/1748-0221/13/03/C03015  
one may ask what the added scientific value of the presented article is. In any case these papers have to be referenced.

**A4**: These two paper have been referenced in the manuscript for performance comparison. The relevant parts are written as below:

“The curve was fitted by a complementary error function, the centre value corresponds to the charge threshold and the sigma parameter represents the noise-induced width. The results of the curve is closed to the previous work finished by T. Suehara [14].”

“The system is based on the prior work performed within the CALICE collaboration, using their ASIC and referencing to the readout electronics architecture of the CALICE ECAL physics prototype and technical prototype [5,6].”

[6] Amjad M S et al., Beam test performance of the SKIROC2 ASIC, Nucl. Instrum. Meth. A 778 (2015) 78.

[14] T. Suehara et al., Performance study of SKIROC2/A ASIC for ILD Si-W ECAL, 2018 JINST 13(03) C03015

Speaking of the scientific value, although the same work has been done by CALICE collaboration for ILD, there is no such study for Si-W ECAL of CEPC in China. The work introduced in the manuscript is the first step for the Si-W ECAL prototype of CEPC, according to pre-CDR put forward in 2015.

**Q5:** on THE SKIROC2  
at THE Circular  
through A gigabit  
1. Introduction  
Collider CONCEIVEED to produce  
and making precise ->and to make precise  
taus ->tau leptons  
the high-granularity plays ->the high granularity plays  
critical role in determining the maximum capability of particle separation

->critical role in the capability of particle separation

\*\*\* At the end of the section, it should be mentioned that also experiments at other future electron positron colliders have studied a silicon-tungsten based ECAL, and the ILC TDR and CLIC CDR be quoted. This would also better explain why their results are being quoted in the paragraph below. A mentioning of and reference to the CMS endcap calorimeter upgrade would also be appropriate

**A5**: These grammatical errors above have been corrected as comments recommend.

The three papers have been quoted at the end of the section. This section has been rewritten as below:

“The high granularity plays a critical role in the capability of particle separation and silicon-tungsten-based ECAL (Si-W ECAL) is considered as a promising candidate for this type of applications. There are experiments at other future electron positron colliders which have studied silicon-tungsten-based ECAL [3,4]. The CMS endcap calorimeter upgrade also used full granularity of the calorimeter to replace the old one [5].”

[3] T. Behnke et al., The International Linear Collider Technical Design Report - Volume 4: Detectors, [arXiv:1306.6329].

[4] L. Linssen, A. Miyamoto, M. Stanitzki and H. Weerts (eds), Physics and Detectors at CLIC: CLIC Conceptual Design Report, <http://cds.cern.ch/record/1425915CERN-2012-003>.

[5] CMS collaboration. Projected Performance of an Upgraded CMS Detector at the LHC and HL-LHC: Contribution to the Snowmass Process, [arXiv:1307.7135].

**Q6**: Results of THE CALICE ECAL  
For THE international  
Tens of millions OF electronic channels  
Dozens of layers ->give exact number  
\*\*\* Minimal power (<10mW per channel). This requirement is considered to be sufficient for linear colliders with their low duty cycle, because one can cycle the power, such that few 10s or micro-Watts per channel result. This is not possible at a circular collider, and it is the main difference in requirements for the calorimeter concept. So it should be discussed with a few sentences. It would be surprising if 10 mW per channel is sufficient to operate the detector without cooling

**A6:** These grammatical errors above have been corrected as comments recommend.

You are right that the CEPC is quite different from linear collider on the requirements for cooling. Since it works in continuous mode, the power-pulsed operation mode can not be used. The power consumption should much lower than that of linear collider. This part has been rewritten like this:

“In addition, the high-level integration should be carried out with minimal power consumption. Different from linear collider, the CEPC is not able to work in the power-pulsed operation mode, which means the power consumption should be much lower than that of linear collider for thermal requirements (at least lower than 1 mW / channel).”

**Q7**: System  
data to A PC  
earlier, there were dozens of layers, now it is 6. Is this the first stage of a  
larger prototype? Please clarify.  
SKIROC2 was developed in the CALICE collaboration, as is stated in [7];  
please mention.  
CSA ->SCA, several times.  
The total active area is 5x5mm2 ->the active area of one cell is 5x5mm2  
Low power rejection (82 dB) ->of 82 dB  
Output noise (4 uV rms) -? Output noise rms of 4 uV

**A7:** These grammatical errors above have been corrected as comments recommend.

The system has two stages. Stage one is to put forward a small system (with several layers) for basic performance test. Stage two is to expand the system to a beam prototype without changing the interface protocol. This part has been added to the manuscript:

“At the first stage, a small system with several layer of silicon PIN array will be designed. The system is for basic performance test such as noise and calibration of single channel. The system should also have potential for expansion without changing the interface protocol.”

The CALICE collaboration has been mentioned in the paper.

“The core of the FEB is the SKIROC2 (Silicon Kalorimeter Integrated ReadOut Chip 2) chip developed in the CALICE collaboration from France [11]”

[11] S. Callier, F. Dulucq, C. de La Taille, G. Martin-Chassard and N. Seguin-Moreau, SKIROC2, front end chip designed to readout the Electromagnetic CALorimeter at the ILC, 2011 JINST 6 C12040

CSA means charge-sensitive amplifier, while SCA is for switched capacitor arrays. The use of CSA is to describe feature of charge-sensitive amplifier. I checked it again and made sure there was not mistake.

**Q8**: \*\*\* Fig 4: Actually one would like to see the entire powering scheme, including the depletion voltage and the input coupling to the pre-amp

**A8**: The figure has been modified and add the input coupling to SKIROC2’s pre-amp.



**Q9:** Convertion ->conversion  
Memory on chip ->on the chip  
Controlled by field-programmable ->by a field-..  
On DIF ->on the DIF

Valid the SCA ->validate the SCA  
Configures 616-bits registers ->configures the 616-bit registers on the chips  
Such as C f and trigger mode ->such as the feed-back capacitance C f and  
the trigger mode  
ASIC on FEB ->ASIC on the FEB  
Transmit them to DIF ->to the DIF  
Expend FEB expand THE FEB  
Interface definition to FEB ->to the FEB  
5V to FEB ->to the FEB.  
The FPGA Is composed of an FPGA ->the FPGA part is  
Function of FPGA ->of the FPGA  
Control FEB ->the FEB  
With DCM ->with the DCM  
Or PC ->or the PC  
In the normal mode ->in normal mode  
Into FPGA ->into the FPGA  
To DCM or PC ->to the DCM or to the PC  
Ex-trigger mode ->external trigger mode  
\*\*\* here an explanation is missing that normally the chip is self-triggered

**A9**: These grammatical errors above have been corrected as comments recommend.

The explanation about self-trigger has been added to the paper.

“The trigger module is in charge of generating a trigger when working in calibration mode or external trigger mode, while normally the chip is self-triggered.”

**Q10**: Which discussed below ->which is discussed below  
From FIFO to DCM ->from the FIFO to the DCM  
Gets a command from DCM ->receives commands from the DCM  
GTP ->what is this?  
On FPGA ->on the FPGA  
\* GTP is not explained  
\* Fig 6 SPP is not explained  
With PC ->with the PC  
As well as initial power supply to FEB ->As well as the initial power supply  
to the FEB  
Generated for DOF˜->for the DIF.  
Data from DIFs ->data from one or several DIFs  
Designed for PandaX ->for the PandaX  
The picture of DCM ->a picture of the DCM  
An FPGA of Zync-7 ->an FPGA of the Zync-7type  
One DCM carries 6 DIFs ->serves 6 DIFs  
\* GTX is not explained

**A10**: These grammatical errors above have been corrected as comments recommend.

GTP and GTX has no special meaning. They are just names for high speed transceiver on FPGA of ARTIX7 and Zynq-7. The relevant parts have been rewritten as these:

“The transmission is based on the high-speed transceiver named GTP on FPGA.” and

“The SFPs are implemented with FPGA-based gigabit transceiver named GTX to read…”

The meaning of SFP in Fig 6 is explained in the section of data interface, below the figure:

“The interface part is composed of a 1 Gbps bidirectional small form-factor pluggable (SFP) optical transceiver…”

**Q11**: Performance of readout system ->the readout system  
\*\*\* Fig 6: both plots have no axis labels  
Acquisition of baseline ->of the baseline  
Required by SKIROC2 ->by the SKIROC2 chip  
SKIROC2 held ->The chip held  
It worth noting ->it is worth noting  
Demonstrated the noise level ->demonstrated a noise level  
\*\*\* Fig 9 has no axis labels either  
Range of SKIROC2 ->range of the SKIROC2 chip  
By taking advantaging of ->advantage of  
From test pulse input ->from the test pulse input  
The SKIROC2 had many ->the SKIROC2 chips has many  
\* Fig 10 caption: The trigger efficiency for two channels as a function of  
threshold setting for an input charge of 2 fC.  
Via the S-curve and presented in Fig ->from an S-curve as presented in Fig.  
With 4-but DAC ->with a 4-bit DAC  
Exceeded the threshold .. would output ->exceeds the threshold .. the  
SKIROC2 chip generates a trigger signal  
Where center value ->the center value  
the threshold on the charge and the sigma represents the noise power -  
>the charge threshold and the sigma parameter represents the noise-induced  
width.  
In newer version ->in a newer version  
With X-ray source ->with an X-ray source

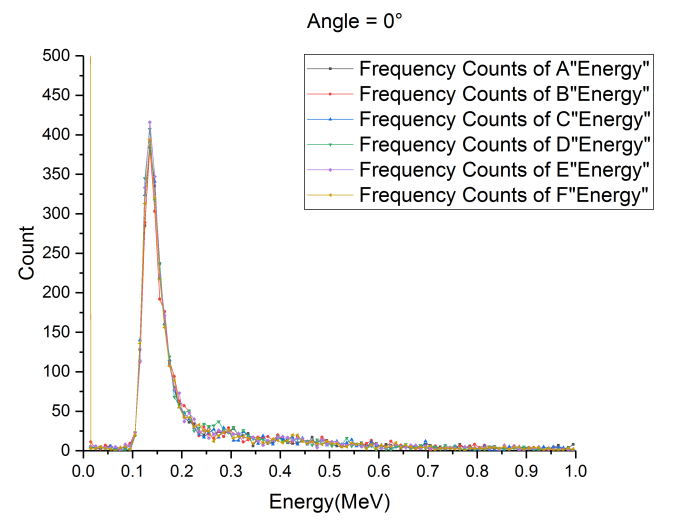
**A11**: These grammatical errors above have been corrected as comments recommend.

There were some bugs when converting original word file into pdf. Leading to the result that some axis labels missed. I used .jpg instead of previous visio file and solved this problem.

**Q12**: \*\*\* The bias voltage of 13 V appears to be too low for a full depletion of the wafer with 400 micron thickness. The CALICE prototype paper [5] reports 150V for a 500 micron wafer. Possibly a thin depletion layer is sufficient for the registration of X-ray signals, if irradiated from the right side. However, this raises the question how representative the S/N results are. This should be discussed.

**A12**: The maximum reverse voltage of silicon PIN diode S5980 is 30 V, according to the datasheet of HAMAMATSU. I was also curious about why the bias voltage had so much difference from that of CALICE prototype and discussed this question with Hamamatsu technicians. They told me that the CALICE silicon PIN arrays were customized and had special demands for dark current and thermal capacitance. In order to satisfy the demands, HAMAMATSU used different materials and production process, leading to the fact that the bias voltage is much larger than S5980’s.

Besides, I have done cosmic ray simulation about this kind of silicon PIN diode S5980 (460 micron thickness) with Geant4. When the cosmic ray perpendicularly incidents the diode, the most probable value of deposited energy is around 145 keV, which stands for 7.3 fC. The test result (7.24 fC) with the system is basically the same with simulation. So I got this conclusion that the 13V bias is OK for S5980.



**Q13**: \*\*\* Fig 11: The line shape is not Gaussian. Should be commented

**A13**: This part has been added to the manuscript to comment why the shape is not Gaussian:

“It can be observed that the shape is not standard Gaussian. This is because there is a certain chance that the photon has photoelectric effect before the depletion layer and losses some energy.”

**Q14:** \*\*\* Fig 12: Cosmic ray test: Has an external trigger been used? Or has a selection (coincidence between layers) been applied? The origin of the 2 contributions in Fig.12 should be explained. In auto-trigger only signals above threshold should be seen. The SKIROC2 output contains the charges of all channels if one has triggered, so it could be non-triggered channels in triggered events.

\*\*\* Moreover, it remains unclear whether the shown pulse height distribution is for a single channel or for several channels. (I assume not, since inter-calibration is not mentioned.

**A14**: You are right that the external trigger has been used. The distribution of Fig 12 was from a single channel. The SKIROC2 was set to work at both in-trigger and ex-trigger mode. The threshold of inner trigger was set at 0.5 MIP. At the same time, a random external trigger was added to get the pedestal noise. That is the origin of the 2 contributions in Fig 12. This part has been added to this section:

“Figure 12 shows the first result obtained with this system. The shown two pulse distribution were from a single channel. The SKIROC2’s trigger threshold was set at 0.5 MIP (with about 5 σ separation of the noise) to get signal from cosmic ray. In addition, there was a random external trigger to get the pedestal noise. ”

**Q15:**\*\*\* The entire characterization section is somewhat disappointing, since uniformity results are shown for a single chip only, and performance results are given for individual channels only. No statements are made on the entire 6-larer system

**A15:** I’m sorry that I failed to clearly explain the main topic of this paper. This is a preliminary study on the prototype (for beam test), focused on the architecture and basic performance. Since this is the first stage, the main task is to verify the feasibility. That’s why the results are for single chip. Thanks to the encouraging results elaborated in the paper, the second stage is in progress. In the second stage, the newer version of FEB will integrate more ASICs and silicon PIN cells for beam test, the next DCM will also be designed.

**Q16**: Based on SKIROC2 ->based on the SKIROC2  
\*\*\* System is scalable: This is over-selling the results. The system may be scalable to a test beam prototype like the one constructed by CALICE in 2005, but since the electronics is still external and next to instead of on top of the wafer, it is not scalable to a collider detector

**A16:** This comment was discussed together with Q2.

The grammatical error above has been corrected as recommend.

**Q17**: The performance assessment of the system is discussed in detail. It is discussed on the single channel level, and some results on chip level are given.

**A17**: The related part of Conclusion has been rewritten like this:

“The performance assessment of the system with one single layer is discussed in detail.”